



US 20190341439A1

(19) **United States**(12) **Patent Application Publication**
CHOI et al.(10) **Pub. No.: US 2019/0341439 A1**(43) **Pub. Date: Nov. 7, 2019**(54) **ORGANIC LIGHT-EMITTING DISPLAY
DEVICE**(71) Applicant: **Samsung Display Co., Ltd.**, Yongin-Si
(KR)(72) Inventors: **Yoonsun CHOI**, Hwaseong-si (KR);
Seong Ryong LEE, Hwaseong-si (KR);
Hyun Chul KIM, Hwaseong-si (KR);
Seongjun LEE, Seoul (KR); **Eunae
JUNG**, Hwaseong-si (KR)(21) Appl. No.: **16/377,255**(22) Filed: **Apr. 8, 2019**(30) **Foreign Application Priority Data**

May 4, 2018 (KR) 10-2018-0052158

Publication Classification(51) **Int. Cl.**
H01L 27/32 (2006.01)
H01L 51/52 (2006.01)
G09G 3/3291 (2006.01)(52) **U.S. Cl.**CPC **H01L 27/3276** (2013.01); **H01L 51/5256**
(2013.01); **H01L 27/3246** (2013.01); **G09G**
2300/0439 (2013.01); **G09G 3/3291** (2013.01);
G09G 2300/0426 (2013.01); **H01L 27/323**
(2013.01)(57) **ABSTRACT**

An organic light-emitting display device includes a base substrate, a pixel array, a first power voltage wiring and a second power voltage wiring. The base substrate includes a pixel area and a peripheral area that surrounds the pixel area. The pixel array is disposed in the pixel area. The first power voltage wiring is disposed in the peripheral area and includes a first lower power voltage line and a first upper power voltage line. The first upper power voltage line is disposed on the first lower power voltage line and contacts the first lower power voltage line. The second power voltage wiring is disposed in the peripheral area and includes a second lower power voltage line and a second upper power voltage line. The second upper power voltage line is disposed on the second lower power voltage line and contacts the second lower power voltage line. The first upper power voltage line overlaps the second lower power voltage line in a plan view.

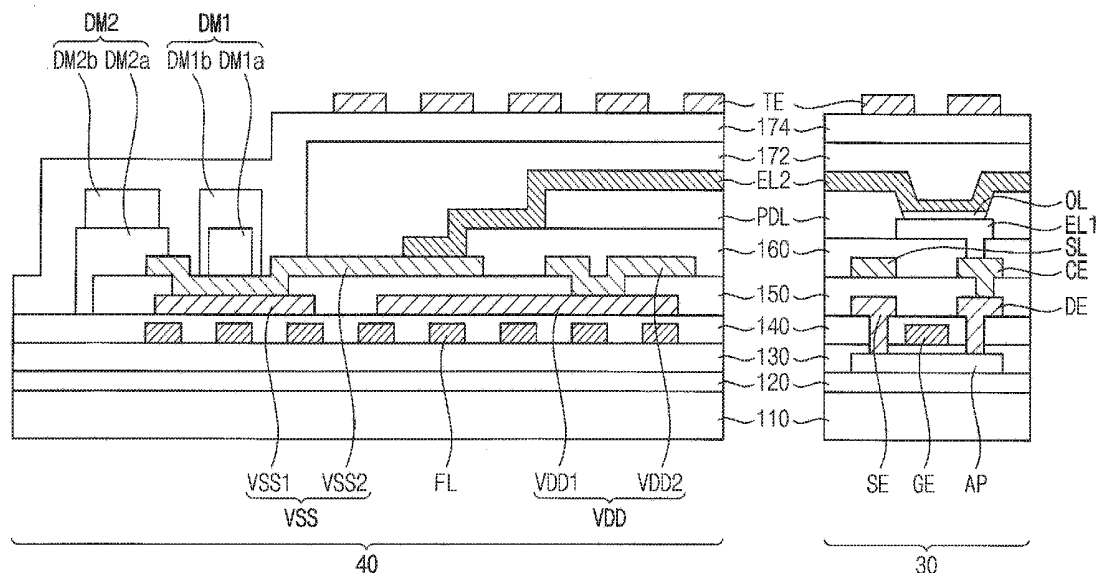


FIG. 1

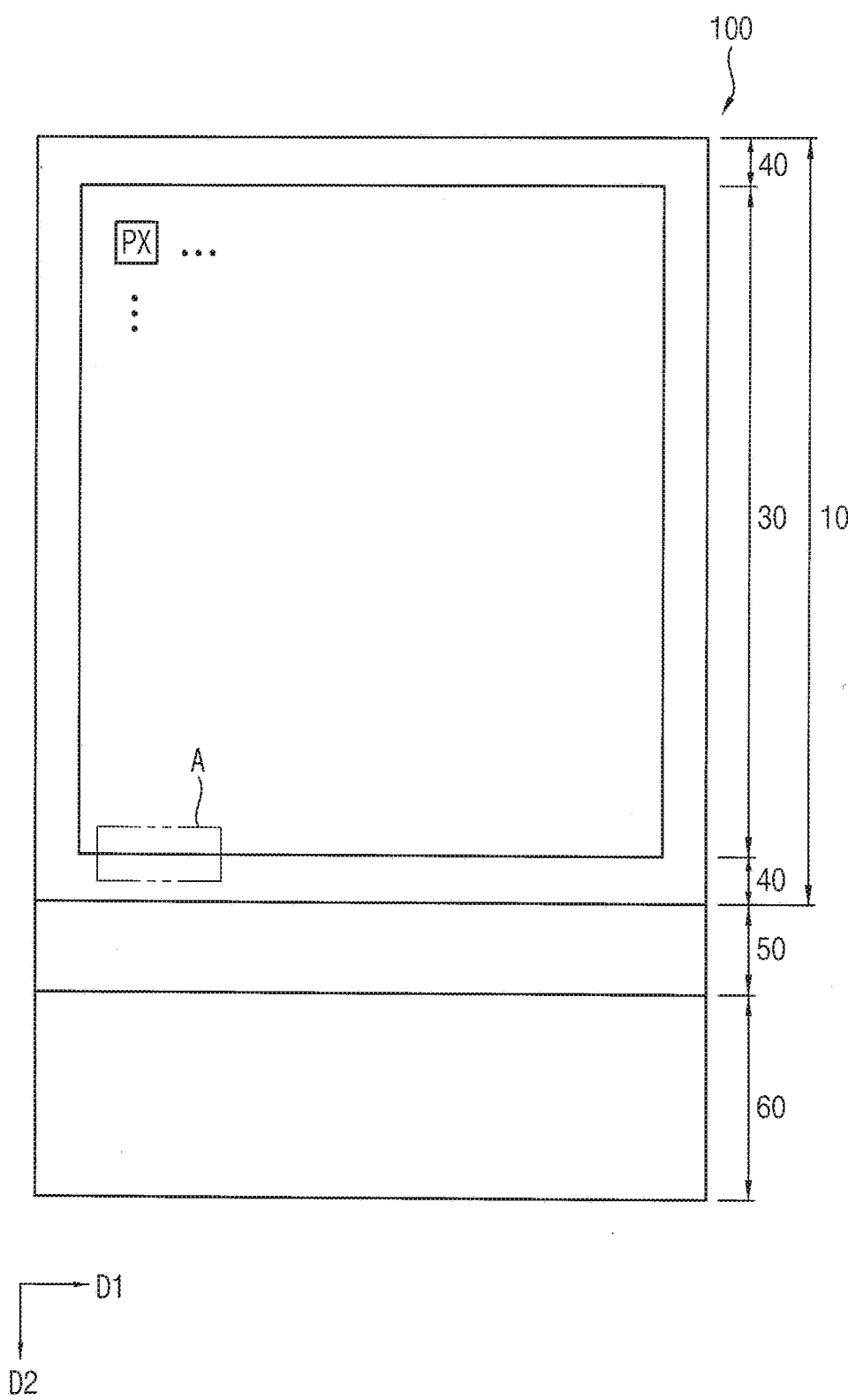


FIG. 2

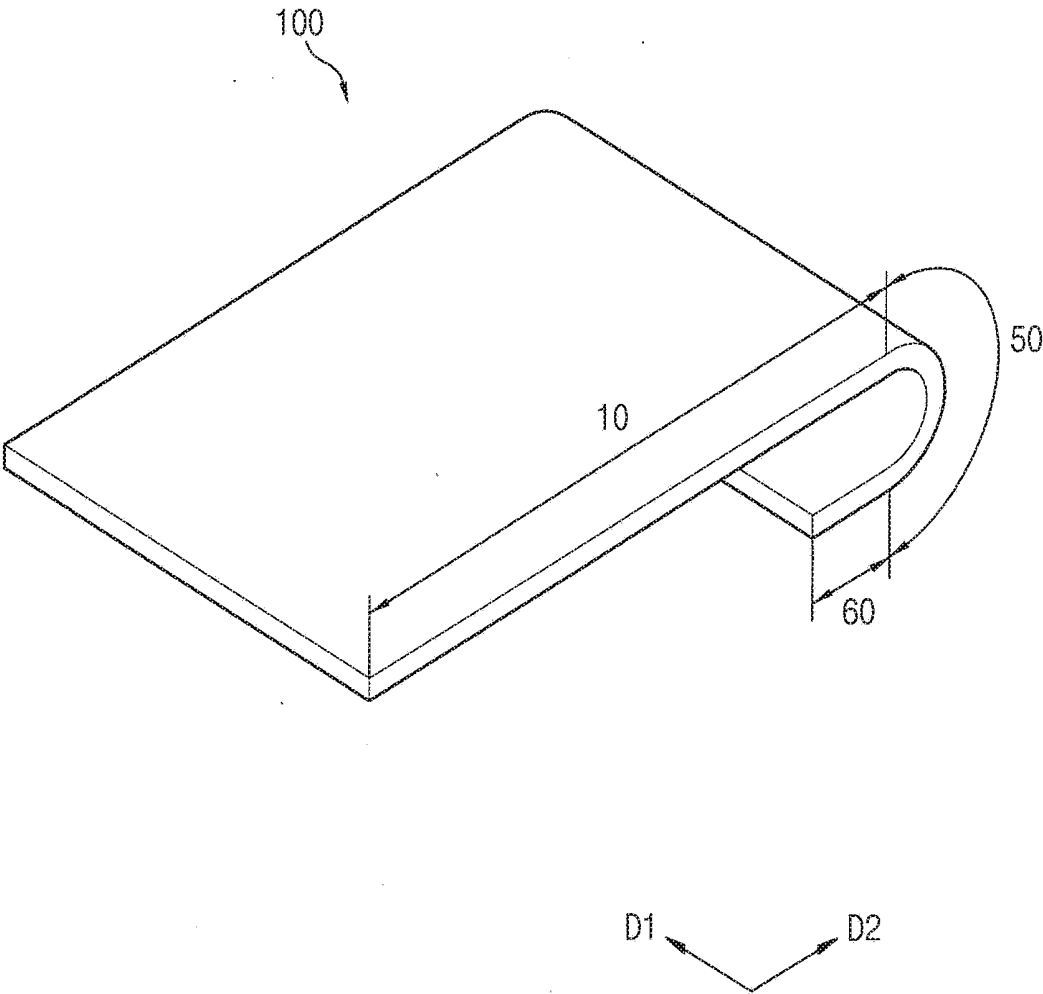


FIG. 3

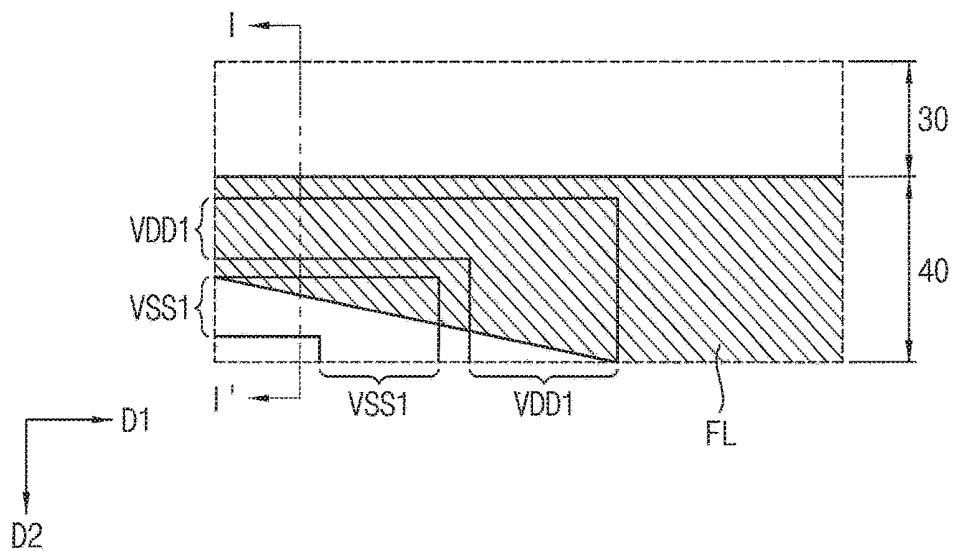


FIG. 4

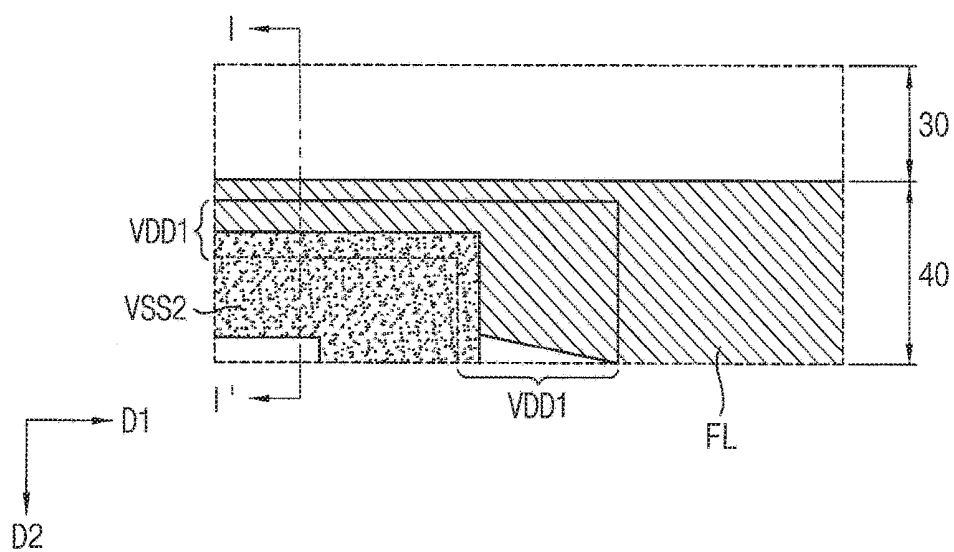


FIG. 5

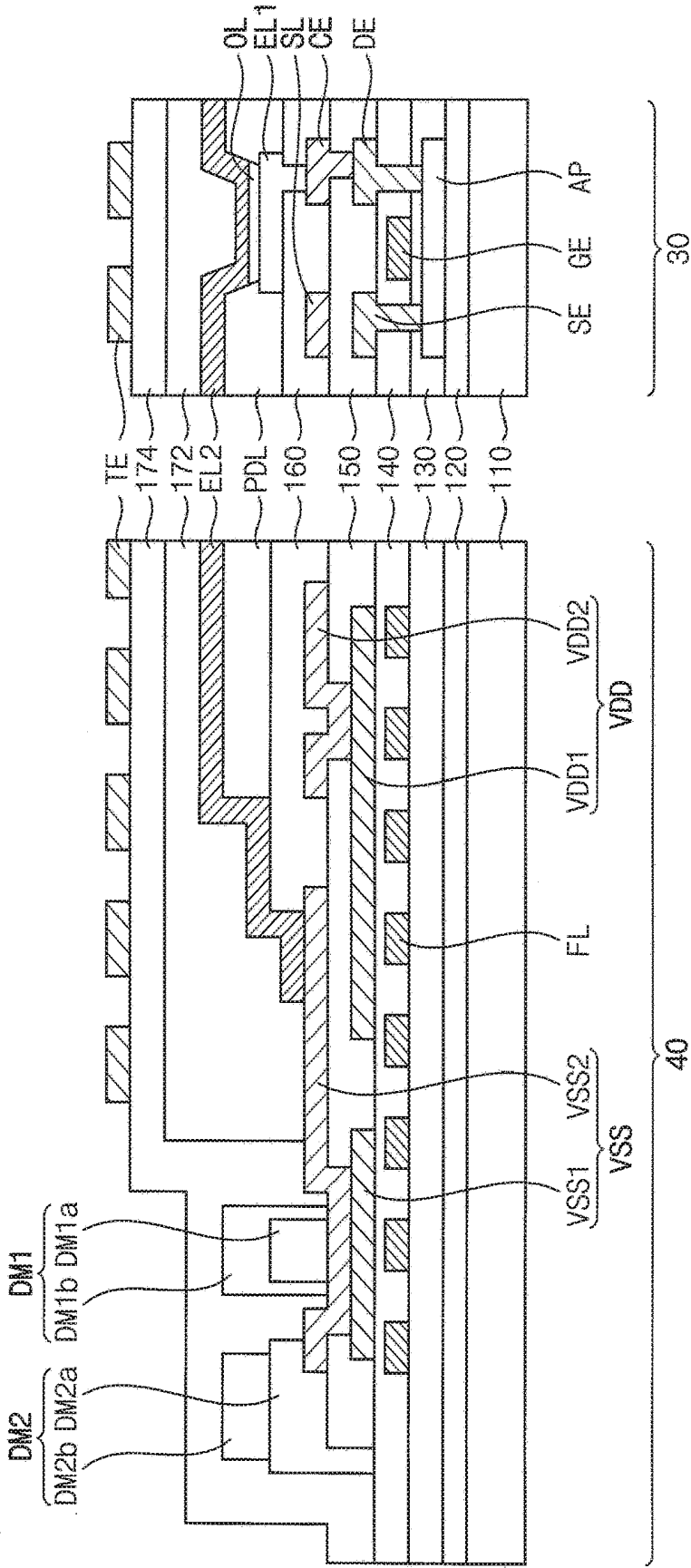


FIG. 6

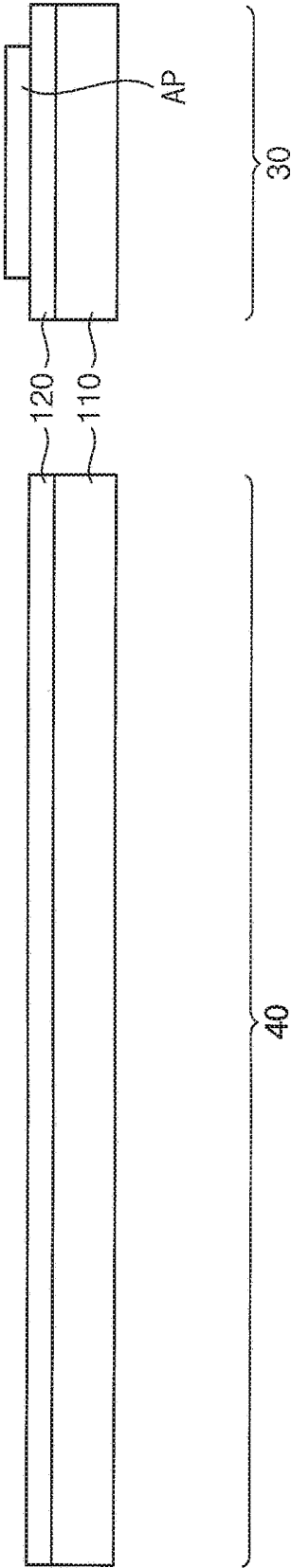


FIG. 7

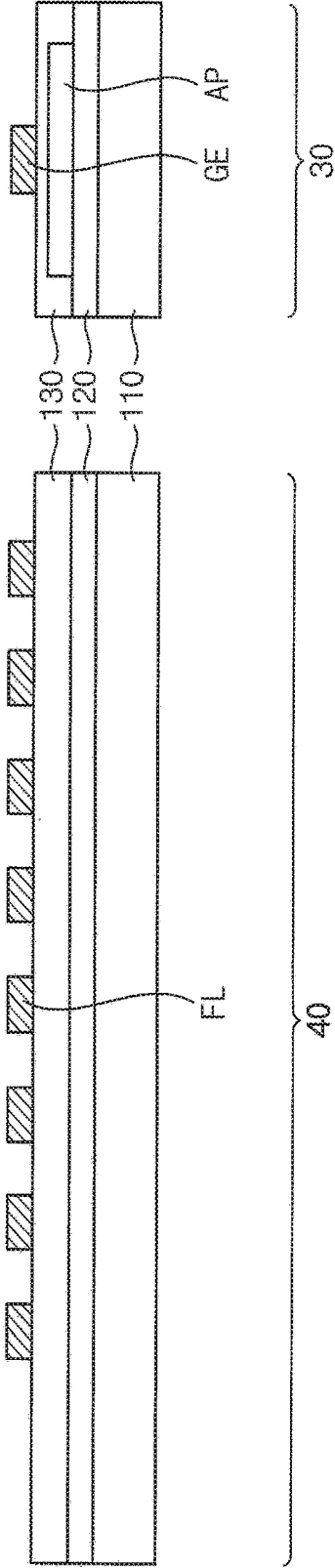


FIG. 8

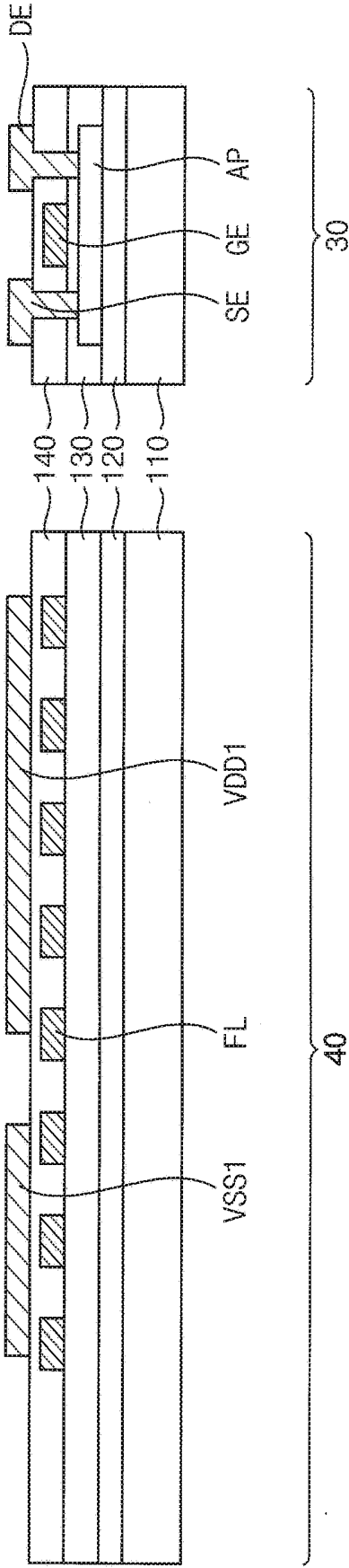


FIG. 9

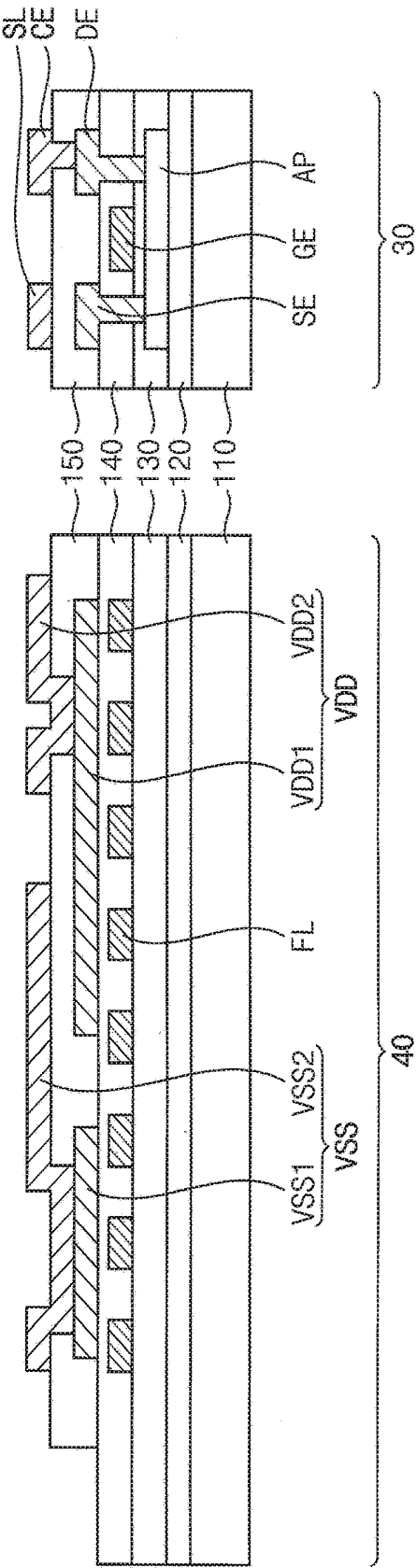


FIG. 10

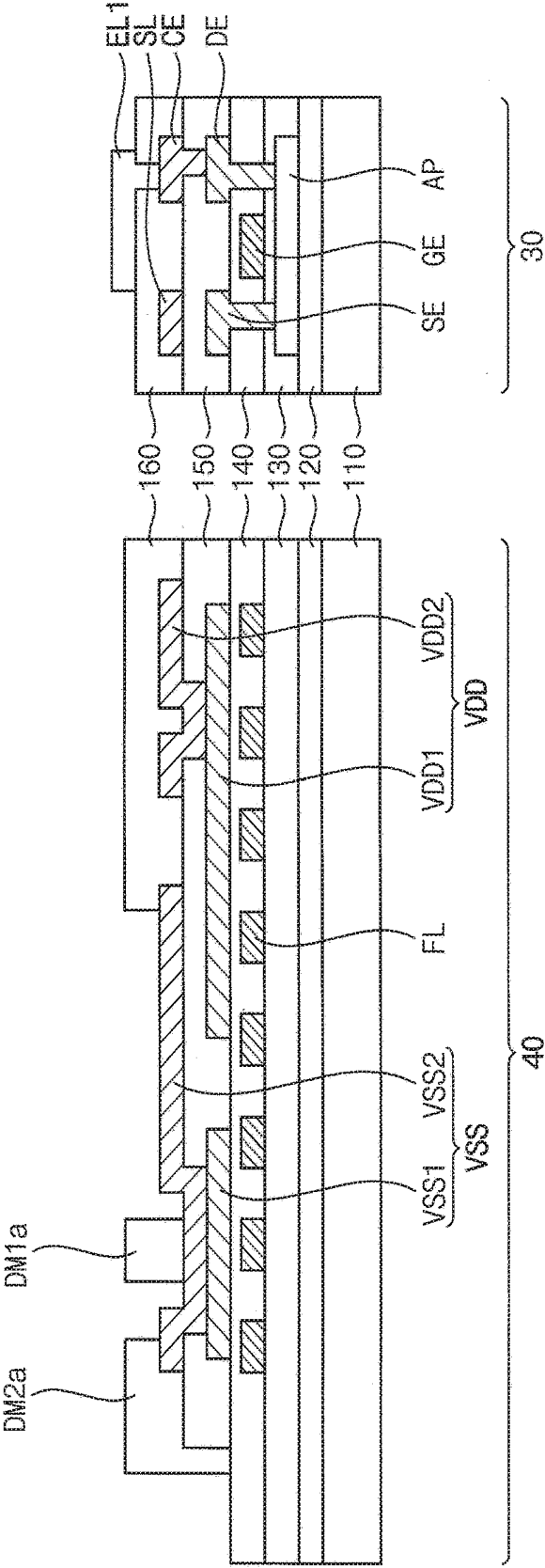


FIG. 12

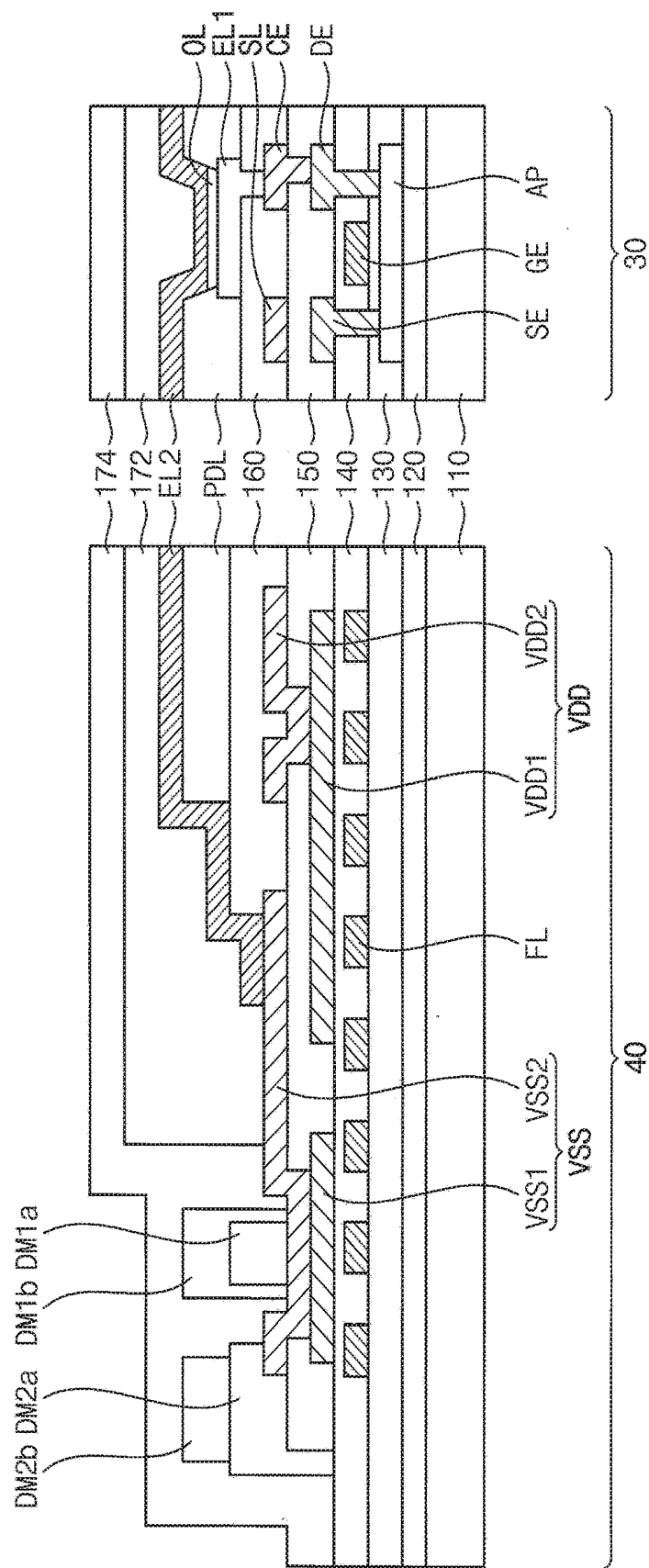


FIG. 13

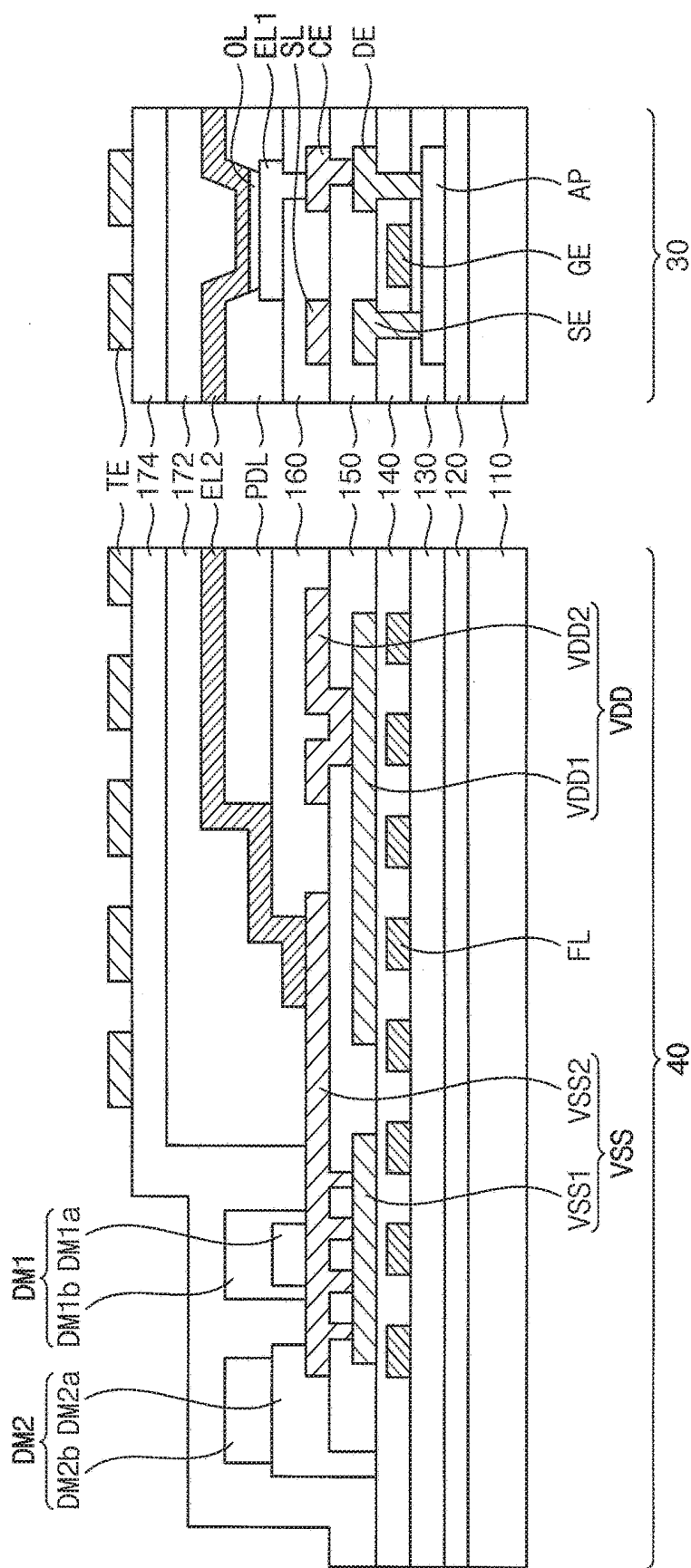
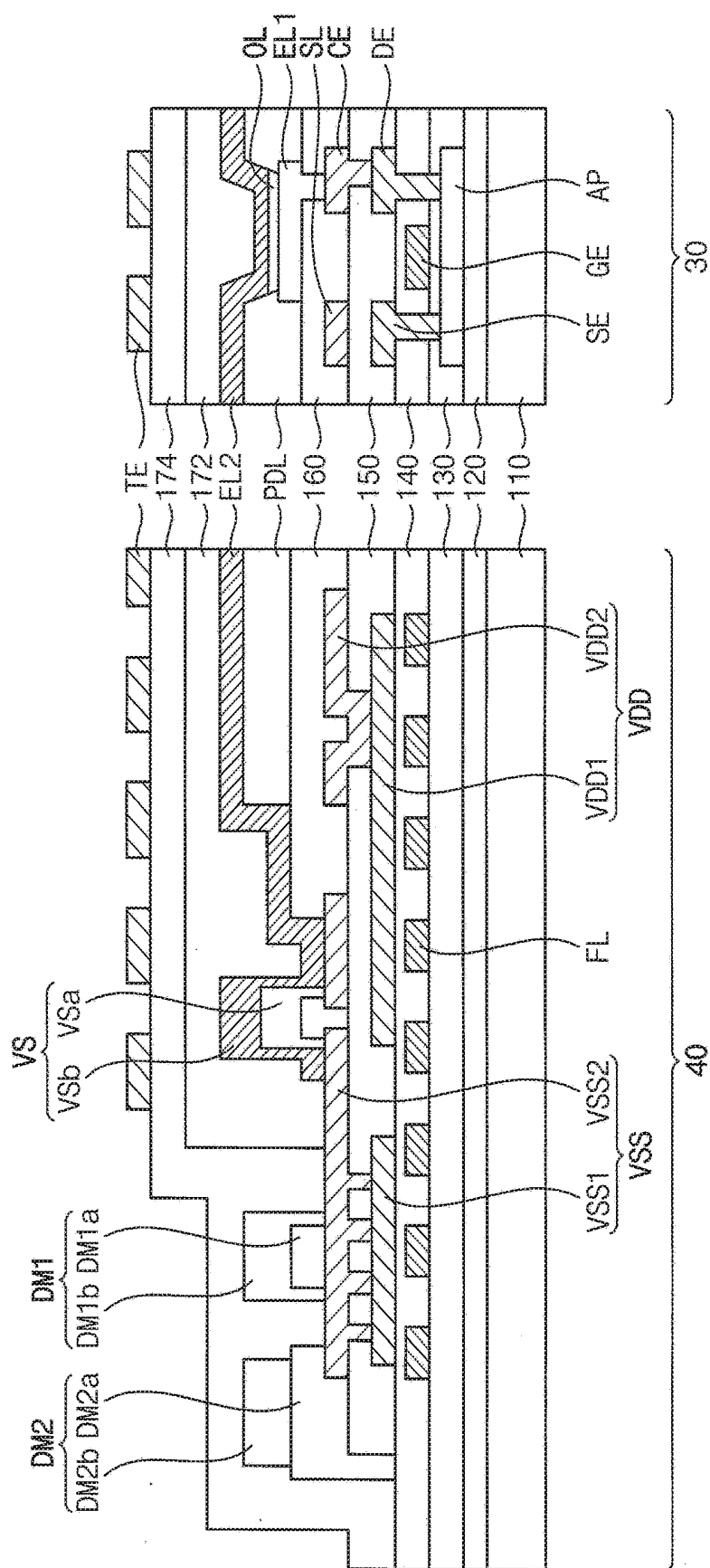


FIG. 14



ORGANIC LIGHT-EMITTING DISPLAY DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to and the benefit of Korean Patent Application No. 10-2018-0052158 filed on May 4, 2018 in the Korean Intellectual Property Office, the entire disclosure of which is incorporated by reference herein in its entirety.

BACKGROUND

1. Field

[0002] Exemplary embodiments of the present disclosure relate to a display device, more particularly, to an organic light-emitting display device.

2. Description of the Related Art

[0003] A flat panel display device has substituted a conventional display device such as a cathode-ray tube display device for its lightweight and relatively thinness. Examples of the flat panel display device include a liquid crystal display (LCD) device and an organic light-emitting display device.

[0004] Recently, a flexible organic light-emitting display device has been researched and developed. The flexible organic light-emitting display device is capable of being bent or folded at least at a portion thereof. For example, the flexible organic light-emitting display device may include a flexible base substrate, a pixel array disposed on the base substrate, and a thin film encapsulation layer covering the pixel array. The flexible organic light-emitting display device may increase visibility and reduce an area size of a non-display area by bending or folding a portion thereof.

SUMMARY

[0005] Exemplary embodiments of the present disclosure provide an organic light-emitting display device.

[0006] According to an exemplary embodiment, an organic light-emitting display device includes a base substrate, a pixel array, a first power voltage wiring and a second power voltage wiring. The base substrate includes a pixel area and a peripheral area that surrounds the pixel area. The pixel array is disposed in the pixel area. The first power voltage wiring is disposed in the peripheral area and includes a first lower power voltage line and a first upper power voltage line. The first upper power voltage line is disposed on the first lower power voltage line and contacts the first lower power voltage line. The second power voltage wiring is disposed in the peripheral area and includes a second lower power voltage line and a second upper power voltage line. The second upper power voltage line is disposed on the second lower power voltage line and contacts the second lower power voltage line. The first upper power voltage line overlaps the second lower power voltage line in a plan view.

[0007] In an exemplary embodiment, the second power voltage wiring is disposed between the first power voltage wiring and the pixel area.

[0008] In an exemplary embodiment, the first lower power voltage line is spaced apart from the second lower power

voltage line, and the first upper power voltage line is spaced apart from the second upper power voltage line.

[0009] In an exemplary embodiment, a width of the first upper power voltage line is greater than a width of the first lower power voltage line, and a width of the second upper power voltage line is smaller than a width of the second lower power voltage line.

[0010] In an exemplary embodiment, the first upper power voltage line covers a gap between the first lower power voltage line and the second lower power voltage line in a plan view.

[0011] In an exemplary embodiment, the pixel array includes an organic light-emitting diode that includes a first electrode and a second electrode. The second electrode of the organic light-emitting diode extends from the pixel area to the peripheral area and contacts the first upper power voltage line.

[0012] In an exemplary embodiment, the organic light-emitting display device further includes a fan-out wiring overlapping the first power voltage wiring and the second power voltage wiring.

[0013] In an exemplary embodiment, the fan-out wiring is disposed under the first power voltage wiring and the second power voltage wiring.

[0014] In an exemplary embodiment, the fan-out wiring includes a plurality of lines spaced apart from each other. At least a portion of the fan-out wiring overlaps a gap between the first lower power voltage line and the second lower power voltage line in a plan view.

[0015] In an exemplary embodiment, the organic light-emitting display device further includes a touch screen structure disposed in the pixel area and the peripheral area to overlap the fan-out wiring.

[0016] In an exemplary embodiment, the fan-out wiring is configured to transfer a data signal to the pixel array.

[0017] In an exemplary embodiment, the organic light-emitting display device further includes a first via insulation layer partially covering the first lower power voltage line and the second lower power voltage line.

[0018] In an exemplary embodiment, the first via insulation layer includes one or more contact holes. The first upper power voltage line is connected to the first lower power voltage line through the one or more contact holes of the first via insulation layer.

[0019] In an exemplary embodiment, the first via insulation layer includes one or more contact holes. The second upper power voltage line is connected to the second lower power voltage line through the one or more contact holes of the first via insulation layer.

[0020] In an exemplary embodiment, the organic light-emitting display device further includes a thin film encapsulation layer covering the pixel array and extending to the peripheral area.

[0021] In an exemplary embodiment, the thin film encapsulation layer includes at least one organic layer and at least one inorganic layer.

[0022] In an exemplary embodiment, the organic light-emitting display device further includes at least one dam structure disposed in the peripheral area.

[0023] In an exemplary embodiment, the organic light-emitting display device further includes at least one valley structure disposed between the at least one dam structure and the pixel area.

[0024] In an exemplary embodiment, the pixel array includes an organic light-emitting diode that includes a first electrode and a second electrode. The second electrode of the organic light-emitting diode is disposed in the pixel area and the peripheral area, extends along a side surface and an upper surface of the at least one valley structure in the peripheral area, and contacts the first upper power voltage line.

[0025] In an exemplary embodiment, the at least one valley structure is disposed on the first upper power voltage line and is connected to a first via insulation layer that is disposed under the first upper power voltage line through a contact hole of the first upper power voltage line.

[0026] According to exemplary embodiments, a first power voltage wiring and a second power voltage wiring that are disposed in a peripheral area include a plurality of lines that are formed in different layers and disposed on different planes, respectively. Thus, the first power voltage wiring and the second power voltage wiring may have a reduced width compared to a single-layered structure in view of conductivity. Thus, a size of the peripheral area may be reduced, and a size of a non-display area in the organic light-emitting display device may be reduced.

[0027] In an exemplary embodiment, the first upper power voltage line expands toward the pixel area, and the second lower power voltage line expands toward the first power voltage wiring thereby forming an asymmetrical structure. Thus, a boundary of the second electrode of the organic light-emitting diode may be shifted toward the pixel area. Accordingly, a size of the second electrode in the peripheral area may be reduced, and a size of the non-display area in the organic light-emitting display device may be reduced.

[0028] In an exemplary embodiment, the first upper power voltage line may cover a gap between the first lower power voltage line and the second lower power voltage line in a plan view. Thus, a noise generated by interference between the fan-out wiring and the touch screen structure may be reduced or prevented.

BRIEF DESCRIPTION OF THE DRAWINGS

[0029] Aspects of one or more exemplary embodiments of the present inventive concept will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings.

[0030] FIG. 1 is a plan view illustrating an organic light-emitting display device according to an exemplary embodiment.

[0031] FIG. 2 is a perspective view illustrating a bent shape of the organic light-emitting display device illustrated in FIG. 1.

[0032] FIGS. 3 and 4 are enlarged plan views illustrating the region 'A' of FIG. 1.

[0033] FIG. 5 is a cross-sectional view taken along the line I-I' of FIGS. 3 and 4.

[0034] FIGS. 6 to 12 are cross-sectional views illustrating an example process of manufacturing the organic light-emitting display device illustrated in FIGS. 1 to 5 according to an exemplary embodiment.

[0035] FIG. 13 is a cross-sectional view illustrating an organic light-emitting display device according to an exemplary embodiment.

[0036] FIG. 14 is a cross-sectional view illustrating an organic light-emitting display device according to an exemplary embodiment.

DETAILED DESCRIPTION

[0037] An organic light-emitting display device and a method of manufacturing the organic light-emitting display device according to exemplary embodiments of the present inventive concept will be described hereinafter with reference to the accompanying drawings, in which some exemplary embodiments are shown. Same or similar reference numerals may be used for same or similar elements in the drawings.

[0038] FIG. 1 is a plan view illustrating an organic light-emitting display device 100 according to an exemplary embodiment. FIG. 2 is a perspective view illustrating a bent shape of the organic light-emitting display device 100 illustrated in FIG. 1.

[0039] Referring to FIGS. 1 and 2, the organic light-emitting display device 100 may include a display area 10, a bending area 50, and a signal-providing area 60. The display area 10 may include a pixel area 30 and a peripheral area 40 that surrounds the pixel area 30. A pixel array including a plurality of pixels PX may be disposed in the pixel area 30. The display area 10 may correspond to a front portion of the organic light-emitting display device 100.

[0040] A plurality of pad electrodes that are electrically connected to an external device may be disposed in the signal-providing area 60. For example, an external device such as a driving chip may be mounted in the signal-providing area 60, or the pad electrodes may be connected to an external device through a flexible printed circuit board.

[0041] The pixel array may generate a light based on electrical signals provided by the external device to display an image in the display area 10.

[0042] The bending area 50 may be disposed between the display area 10 and the signal-providing area 60. The display area 10, the bending area 50, and the signal-providing area 60 may be arranged sequentially. Connection wirings may be disposed in the bending area 50 to transfer the electrical signals from the signal-providing area 60 to the peripheral area 40.

[0043] A plurality of signal wirings may be disposed in the peripheral area 40 to transfer the electrical signals to the pixel area 30. For example, the signal wirings may transfer a data signal, a scan signal, a light-emitting signal, a power voltage signal, a touch-sensing signal, or the like. Furthermore, a scan driver, a data driver, or the like may be disposed in the peripheral area 40.

[0044] Referring to FIG. 1, a width of the peripheral area 40 that surrounds the pixel area 30 may be uniform. That is, the width of the peripheral area 40 is the same along the perimeter of the organic light-emitting display device 100. However, exemplary embodiments are not limited thereto, and the peripheral area 40 may have various configurations, shapes, and sizes according to a desired design of the organic light-emitting display device 100.

[0045] Referring to FIG. 2, the bending area 50 may bend with respect to an axis along a first direction D1 so that the signal-providing area 60 may be disposed under the display area 10 to overlap at least a portion of the display area 10. Thus, the bending area 50 may have a bent shape after the bending area 50 is bent.

[0046] FIGS. 3 and 4 are enlarged plan views illustrating the region 'A' of FIG. 1. Particularly, FIG. 3 shows a first lower power voltage line VSS1, a second lower power voltage line VDD1, and a fan-out wiring FL that are disposed in the peripheral area 40. FIG. 4 shows a first upper

power voltage line VSS2, the second lower power voltage line VDD1, and the fan-out wiring FL.

[0047] Referring to FIG. 3, the first lower power voltage line VSS1, the second lower power voltage line VDD1, and the fan-out wiring FL may be disposed in the peripheral area 40. The first lower power voltage line VSS1 and the second lower power voltage line VDD1 may be formed in the same layer. Thus, the first lower power voltage line VSS1 and the second lower power voltage line VDD1 may be spaced apart from each other. In an exemplary embodiment, the first lower power voltage line VSS1 may substantially extend in the first direction D1 along the peripheral area 40. The second lower power voltage line VDD1 may be disposed between the first lower power voltage line VSS1 and the pixel area 30. The second lower power voltage line VDD1 may substantially extend in the same direction as the first lower power voltage line VSS1.

[0048] The fan-out wiring FL may be disposed in a different layer from the first lower power voltage line VSS1 and the second lower power voltage line VDD1. In an exemplary embodiment, the fan-out wiring FL may be disposed below the first lower power voltage line VSS1 and the second lower power voltage line VDD1 overlapping at least a portion of the first lower power voltage line VSS1 and the second lower power voltage line VDD1. The fan-out wiring FL may be electrically connected to the pixel array in the pixel area 30 to provide electrical signals to the pixels PX in the pixel area 30. For example, the fan-out wiring FL may transfer a data signal to the pixel array in the pixel area 30.

[0049] Referring to FIG. 4, the first upper power voltage line VSS2 is disposed on the first lower power voltage line VSS1. The first upper power voltage line VSS2 contacts and is electrically connected to the first lower power voltage line VSS1. Furthermore, the first upper power voltage line VSS2 may expand toward the pixel area 30 from the first lower power voltage line VSS1 to overlap a portion of the second lower power voltage line VDD1. Thus, the first upper power voltage line VSS2 may have a shape covering a gap between the first lower power voltage line VSS1 and the second lower power voltage line VDD1 in a plan view.

[0050] Although not illustrated in FIG. 3, a second upper power voltage line VDD2 may be disposed on the second lower power voltage line VDD1. The second upper power voltage line VDD2 contacts and is electrically connected to the second lower power voltage line VDD1. The second upper power voltage line VDD2 may be formed in the same layer as the first upper power voltage line VSS2. Thus, the second upper power voltage line VDD2 and the first upper power voltage line VSS2 may be spaced apart from each other. The above-described structure including the second upper power voltage line VDD2 will be more fully described in the following.

[0051] FIG. 5 is a cross-sectional view taken along the line I-I' of FIGS. 3 and 4.

[0052] Referring to FIG. 5, a pixel PX disposed in the pixel area 30 may include a driving transistor disposed on a base substrate 110, an organic light-emitting diode (OLED) that is electrically connected to the driving transistor, and a thin film encapsulation layer that covers the organic light-emitting diode. The driving transistor may include an active pattern AP, a gate electrode GE that overlaps the active pattern AP, a source electrode SE that is electrically connected to the active pattern AP, and a drain electrode DE that

is electrically connected to the active pattern AP and spaced apart from the source electrode SE.

[0053] The base substrate 110 may include glass, quartz, silicon, a polymer, or the like. For example, the polymer may include polyethylene terephthalate, polyethylene naphthalate, polyether ketone, polycarbonate, polyarylate, polyether sulfone, polyimide, or any combination thereof.

[0054] A buffer layer 120 may be disposed on the base substrate 110. The buffer layer 120 may prevent or reduce penetration of impurities, humidity, or external gas from underneath of the base substrate 110, and may planarize an upper surface of the base substrate 110. For example, the buffer layer 120 may include an inorganic material such as oxide and nitride.

[0055] The active pattern AP may be disposed on the buffer layer 120. The active pattern AP may overlap the gate electrode GE.

[0056] The active pattern AP may include a semiconductor material such as amorphous silicon, polycrystalline silicon (polysilicon), and oxide semiconductor. For example, when the active pattern AP includes polysilicon, at least a portion of the active pattern AP may be doped with impurities, for example, n-type impurities or p-type impurities.

[0057] A first insulation layer 130 may be disposed on the active pattern AP. The first insulation layer 130 may include silicon oxide, silicon nitride, silicon oxynitride, silicon carbide, silicon oxycarbide, or any combination thereof. Furthermore, the first insulation layer 130 may include an insulating metal oxide such as aluminum oxide, tantalum oxide, hafnium oxide, zirconium oxide, and titanium oxide. The first insulation layer 130 may have a single-layer structure or a multiple-layer structure including silicon nitride and/or silicon oxide.

[0058] The gate electrode GE may be disposed on the first insulation layer 130. The gate electrode GE may include gold (Au), silver (Ag), aluminum (Al), copper (Cu), nickel (Ni), platinum (Pt), magnesium (Mg), chromium (Cr), tungsten (W), molybdenum (Mo), titanium (Ti), tantalum (Ta), or any alloy thereof, and may have a single-layer structure or a multiple-layer structure including different metal layers.

[0059] A second insulation layer 140 may be disposed on the gate electrode GE and the first insulation layer 130. The second insulation layer 140 may include silicon oxide, silicon nitride, silicon oxynitride, silicon carbide, silicon oxycarbide, or any combination thereof. Furthermore, the second insulation layer 140 may include an insulating metal oxide such as aluminum oxide, tantalum oxide, hafnium oxide, zirconium oxide, and titanium oxide.

[0060] A source electrode SE and a drain electrode DE may be disposed on the second insulation layer 140. The source electrode SE and the drain electrode DE may be electrically connected to the active pattern AP via respective contact holes that pass through the first insulation layer 130 and the second insulation layer 140. The source electrode SE and the drain electrode DE may include gold (Au), silver (Ag), aluminum (Al), copper (Cu), nickel (Ni), platinum (Pt), magnesium (Mg), chromium (Cr), tungsten (W), molybdenum (Mo), titanium (Ti), tantalum (Ta), or any alloy thereof, and may have a single-layer structure or a multiple-layer structure including different metal layers.

[0061] A third insulation layer 150 may be disposed on the second insulation layer 140 to cover the source electrode SE and the drain electrode DE. The third insulation layer 150 may include an inorganic insulation material, an organic

insulation material, or any combination thereof. Examples of the organic insulation material may include polyimide, polyamide, acrylic resin, phenol resin, and benzocyclobutene (BCB).

[0062] A source line SL and a connection electrode CE may be disposed on the third insulation layer **150**. The source line SL may transfer a scan signal, a data signal, a light-emitting signal, an initialization signal, a power voltage, or the like to transistors of the pixel array. The connection electrode CE may be electrically connected to the drain electrode DE via a contact hole that passes through the third insulation layer **150**. The connection electrode CE may electrically connect the drain electrode DE to a first electrode EL1 of the organic light-emitting diode. The source line SL and the connection electrode CE may include the same material as the source electrode SE and the drain electrode DE.

[0063] A fourth insulation layer **160** may be disposed on the third insulation layer **150** to cover the source line SL and the connection electrode CE. For example, the fourth insulation layer **160** may include an inorganic insulation material, an organic insulation material, or any combination thereof. For example, the organic insulation material may include polyimide, polyamide, acrylic resin, phenol resin, benzocyclobutene (BCB) or the like.

[0064] The first electrode EL1 of the organic light-emitting diode may be disposed on the fourth insulation layer **160**. In an exemplary embodiment, the first electrode EL1 may function as an anode. The first electrode EL1 may be formed as a transmitting electrode or a reflecting electrode according to an emission type of the organic light-emitting diode. When the first electrode EL1 is a transmitting electrode, the first electrode EL1 may include indium tin oxide, indium zinc oxide, zinc tin oxide, indium oxide, zinc oxide, tin oxide, or the like. When the first electrode EL1 is a reflecting electrode, the first electrode EL1 may include gold (Au), silver (Ag), aluminum (Al), copper (Cu), nickel (Ni), platinum (Pt), magnesium (Mg), chromium (Cr), tungsten (W), molybdenum (Mo), titanium (Ti), or any combination thereof, and may have a stack structure further including a material that may be used for the transmitting electrode.

[0065] A pixel-defining layer PDL may be disposed on the fourth insulation layer **160**. The pixel-defining layer PDL may include an opening that exposes at least a portion of the first electrode EL1. The pixel-defining layer PDL may include an organic insulation material.

[0066] An organic light-emitting layer OL may be disposed on the first electrode EL1. In an exemplary embodiment, the organic light-emitting layer OL may be disposed in the opening of the pixel-defining layer PDL. In another exemplary embodiment, the organic light-emitting layer OL may extend over an upper surface of the pixel-defining layer PDL, or may continuously extend across a plurality of pixels PX in the pixel area **30**.

[0067] The organic light-emitting layer OL may include at least a light-emitting layer, and may further include at least one of a hole injection layer (HIL), a hole transporting layer (HTL), an electron transporting layer (ETL), and an electron injection layer (EIL). The organic light-emitting layer OL may include a low molecular weight organic compound or a high molecular weight organic compound.

[0068] In an exemplary embodiment, the organic light-emitting layer OL may emit a red light, a green light, or a blue light. In another exemplary embodiment, the organic

light-emitting layer OL may emit a white light. The organic light-emitting layer OL emitting a white light may have a multiple-layer structure including a red light-emitting layer, a green light-emitting layer, and a blue light-emitting layer, or a single-layer structure including a mixture of a red light-emitting material, a green light-emitting material, and a blue light-emitting material.

[0069] A second electrode EL2 of the organic light-emitting diode may be disposed on the organic light-emitting layer OL. The second electrode EL2 may continuously extend across a plurality of pixels PX on the pixel area **30**.

[0070] In an exemplary embodiment, the second electrode EL2 may function as a cathode. The second electrode EL2 may be formed as a transmitting electrode or a reflecting electrode according to an emission type of the organic light-emitting diode. For example, when the second electrode EL2 is a transmitting electrode, the second electrode may include lithium (Li), calcium (Ca), lithium fluoride (LiF), aluminum (Al), magnesium (Mg), or any combination thereof, and the organic light-emitting display device **100** may further include a sub electrode or a bus electrode line that includes indium tin oxide, indium zinc oxide, zinc tin oxide, indium oxide, zinc oxide, tin oxide, or the like.

[0071] A thin film encapsulation layer may be disposed on the second electrode EL2. The thin film encapsulation layer may have a stack structure of an inorganic layer **174** and an organic layer **172**. In this case, the organic layer **172** may be disposed on the second electrode EL2, and the inorganic layer **174** may be disposed on the organic layer **172**. However, exemplary embodiment are not limited thereto. For example, the thin film encapsulation layer may have a stack structure including one or more of a first inorganic layer, an organic layer and a second inorganic layer, a stack structure including a first inorganic layer, a first organic layer, a second inorganic layer, a second organic layer, and a third inorganic layer.

[0072] In an exemplary embodiment, the organic layer **172** may include a cured resin such as poly(meth)acrylate. For example, the cured resin may be formed by cross-linking reaction of monomers.

[0073] In an exemplary embodiment, the inorganic layer **174** may include an inorganic material such as silicon oxide, silicon nitride, silicon carbide, aluminum oxide, tantalum oxide, hafnium oxide, zirconium oxide, and titanium oxide.

[0074] Although not illustrated, a capping layer and a blocking layer may be disposed between the second electrode EL2 and the thin film encapsulation layer.

[0075] The capping layer may protect the organic light-emitting diode and may promote the light generated by the organic light-emitting diode to exit outwardly.

[0076] In an exemplary embodiment, the capping layer **184** may include an inorganic material or an organic material. Examples of the inorganic material may include zinc oxide, tantalum oxide, zirconium oxide, and titanium oxide. Examples of the organic material may include poly(3,4-ethylenedioxythiophene), PEDOT, 4,4'-bis[N-(3-methylphenyl)-N-phenylamino]biphenyl(TPD), 4,4',4''-tris[(3-methylphenyl)phenylamino]triphenylamine (m-MTDATA), 1,3,5-tris[N,N-bis(2-methylphenyl)-amino]-benzene (o-MTDAB), and 1,3,5-tris[N,N-bis(3-methylphenyl)-amino]-benzene (m-MTDAB).

[0077] The blocking layer may be disposed on the capping layer. The blocking layer may prevent a damage to the organic light-emitting diode by plasma or the like in later

processes. The blocking layer may include lithium fluoride, magnesium fluoride, calcium fluoride, or the like.

[0078] A touch screen structure may be disposed on the thin film encapsulation layer. The touch screen structure may include a sensing electrode TE. In an exemplary embodiment, the touch screen structure may include any combination of the sensing electrode TE and a sub-sensing electrode. The touch screen structure may be of a mutual capacitance type. For example, an external device may provide touch sensing signals to the sensing electrode TE and the sub-sensing electrode. When a user contacts an area corresponding to the sensing electrode TE, capacitance between the sensing electrode TE and the sub-sensing electrode may change. The external device may sense the capacitance variance caused by the user's touch thereby detecting a touch position.

[0079] The fan-out wiring FL, a first power voltage wiring VSS, a second power voltage wiring VDD, a first dam structure DM1 and a second dam structure DM2 may be disposed in the peripheral area 40. The dam structures DM1 and DM2 may extend along the peripheral area 40, for example, in a second direction D2.

[0080] In the peripheral area 40, the buffer layer 120 may be disposed on the base substrate 110, and the first insulation layer 130 may be disposed on the buffer layer 120. The buffer layer 120 and the first insulation layer 130 may extend from the pixel area 30 to the peripheral area 40. The fan-out wiring FL may be disposed on the first insulation layer 130.

[0081] The fan-out wiring FL may be formed in the same layer as the gate electrode GE. Thus, the fan-out wiring FL and the gate electrode GE may be included in a gate metal pattern.

[0082] The fan-out wiring FL may have a shape extending in a direction, and a plurality of lines may be spaced apart from each other as illustrated in FIGS. 3 and 4.

[0083] The second insulation layer 140 covers the fan-out wiring FL.

[0084] The first lower power voltage line VSS1 and the second lower power voltage line VDD1 may be disposed on the second insulation layer 140.

[0085] The first lower power voltage line VSS1 and the second lower power voltage line VDD1 may be formed in the same layer as the source electrode SE and the drain electrode DE, and may be spaced apart from each other in a horizontal direction in a cross-sectional view. The second lower power voltage line VDD1 may be disposed between the first lower power voltage line VSS1 and the pixel area 30.

[0086] The first lower power voltage line VSS1 and the second lower power voltage line VDD1 may overlap the fan-out wiring FL.

[0087] The third insulation layer 150 may partially cover the first lower power voltage line VSS1 and the second lower power voltage line VDD1.

[0088] The first upper power voltage line VSS2 and the second upper power voltage line VDD2 may be disposed on the third insulation layer 150. The first upper power voltage line VSS2 contacts the first lower power voltage line VSS1, and the second upper power voltage line VDD2 contacts the second lower power voltage line VDD1.

[0089] The first upper power voltage line VSS2 and the second upper power voltage line VDD2 may be formed in the same layer as the source line SL and the connection electrode CE, and may be spaced apart from each other in a

horizontal direction. Furthermore, the first upper power voltage line VSS2 may overlap a portion of the second lower power voltage line VDD1. Thus, the first upper power voltage line VSS2 may cover a gap between the first lower power voltage line VSS1 and the second lower power voltage line VDD1 in a plan view as illustrated in FIG. 4.

[0090] The fourth insulation layer 160 may cover at least a portion of the first upper power voltage line VSS2 and the second upper power voltage line VDD2. In an exemplary embodiment, the fourth insulation layer 160 may extend from the pixel area 30 to the peripheral area 40 to cover at least an edge of the first upper power voltage line VSS2.

[0091] The second electrode EL2 may extend from the pixel area 30 and may contact the first upper power voltage line VSS2 in the peripheral area 40. Thus, a first power voltage provided by the first power voltage wiring VSS may be transmitted to the second electrode EL2.

[0092] The second power voltage wiring VDD may provide a second power voltage to the pixel PX in the pixel area 30. For example, a transistor of the pixel PX may generate a driving current by using the second power voltage. The driving current may be provided to the organic light-emitting diode of the pixel PX.

[0093] The first dam structure DM1 may be disposed on the first upper power voltage line VSS2. The first dam structure DM1 may be disposed between the second dam structure DM2 and the pixel area 30.

[0094] The first dam structure DM1 may include an upper pattern DM1b and a lower pattern DM1a. The upper pattern DM1b may be formed in the same layer as the pixel-defining layer PDL. The lower pattern DM1a may be formed in the same layer as the fourth insulation layer 160.

[0095] The second dam structure DM2 may include an upper pattern DM2b and a lower pattern DM2a. The upper pattern DM2b may be formed in the same layer as the pixel-defining layer PDL. The lower pattern DM2a may be formed in the same layer as the fourth insulation layer 160.

[0096] The first dam structure DM1 and the second dam structure DM2 may prevent monomers from overflowing in the process of forming the organic layer 172 of the thin film encapsulation layer.

[0097] In exemplary embodiments, the number of the dam structures is not limited to two, and one or at least three of dam structures may be disposed as desired. Furthermore, the dam structures may be omitted.

[0098] The thin film encapsulation layer may extend from the pixel area 30 to the peripheral area 40. For example, the organic layer 172 may extend to cover at least a portion of the first upper power voltage line VSS2. The inorganic layer 174 may extend to cover the second dam structure DM2.

[0099] The touch screen structure may extend over the thin film encapsulation layer so that the sensing electrode TE may be further disposed in the peripheral area 40.

[0100] In an exemplary embodiment, the first power voltage wiring VSS and the second power voltage wiring VDD respectively include a lower power voltage line and an upper power voltage line that are formed in different layers and disposed on different planes, respectively. Thus, the width of the first power voltage wiring VSS and the second power voltage wiring VDD may be reduced compared to a single-layered power voltage wiring structure to exhibit similar conductivity. Thus, a size (e.g., a width) of the peripheral

area 40 may be reduced, and a size of a non-display area (e.g., a bezel area) in the organic light-emitting display device 100 may be reduced.

[0101] In an exemplary embodiment, the first upper power voltage line VSS2 expands toward the pixel area 30, and the second lower power voltage line VDD1 expands toward the first power voltage wiring VSS thereby forming an asymmetrical structure. Thus, a boundary of the second electrode EL2 of the organic light-emitting diode may be shifted toward the pixel area 30. Accordingly, a size of the second electrode EL2 in the peripheral area 40 may be reduced, and a size of the non-display area in the organic light-emitting display device may be reduced.

[0102] In an exemplary embodiment, the first upper power voltage line VSS2 covers a gap between the first lower power voltage line VSS1 and the second lower power voltage line VDD1 in a plan view. Thus, a noise generated by interference between the fan-out wiring FL and the touch screen structure may be reduced or prevented.

[0103] In an exemplary embodiment, the first power voltage wiring VSS and the second power voltage wiring VDD are disposed in the peripheral area 40 between the pixel area 30 and the bending area 50. However, exemplary embodiments are not limited thereto, and the asymmetrical structure may be applied to various areas where the first power voltage wiring VSS and the second power voltage wiring VDD are disposed.

[0104] FIGS. 6 to 12 are cross-sectional views illustrating an example process of manufacturing the organic light-emitting display device 100 illustrated in FIGS. 1 to 5 according to an exemplary embodiment. FIGS. 6 to 12 show cross-sections taken along the line I-I' of FIGS. 3 and 4.

[0105] Referring to FIG. 6, the buffer layer 120 is formed on the base substrate 110. A semiconductor layer is formed on the buffer layer 120, and patterned to form the active pattern AP in the pixel area 30. The active pattern AP may include polysilicon. For example, an amorphous silicon layer is formed on the buffer layer 120, and a laser may be irradiated onto the amorphous silicon layer to form a polysilicon layer. The polysilicon layer may be further polished as desired.

[0106] Referring to FIG. 7, the first insulation layer 130 is formed to cover the active pattern AP. A gate metal pattern is formed on the first insulation layer 130. In this case, the first insulation layer 130 may be a gate insulation layer.

[0107] The gate metal pattern may include the gate electrode GE disposed in the pixel area 30, and the fan-out wiring FL disposed in the peripheral area 40. The gate electrode GE may overlap the active pattern AP. The fan-out wiring FL may include a plurality of lines extending in a direction and spaced apart from each other. The gate metal pattern may have a single-layer structure or a multiple-layer structure. In an exemplary embodiment, the gate metal pattern may include molybdenum.

[0108] In another exemplary embodiment, at least one additional gate metal pattern may be added in a different layer for forming a double-gate structure and/or a capacitor electrode, and at least one gate insulation layer may be added to cover the additional gate metal pattern.

[0109] Referring to FIG. 8, the second insulation layer 140 is formed to cover the gate metal pattern. Thereafter, a contact hole is formed through the second insulation layer 140 and the first insulation layer 130 to expose a portion of

the active pattern AP. Thereafter, a first source metal pattern is formed on the second insulation layer 140.

[0110] The first source metal pattern may include the source electrode SE, the drain electrode DE, the first lower power voltage line VSS1, and the second lower power voltage line VDD1. The source electrode SE and the drain electrode DE are disposed in the pixel area 30. The source electrode SE and the drain electrode DE are electrically connected to the active pattern AP via respective contact holes that pass through the first insulation layer 130 and the second insulation layer 140, and are spaced apart from each other. The first lower power voltage line VSS1 and the second lower power voltage line VDD1 are disposed in the peripheral area 40, and spaced apart from each other.

[0111] At least one of the first lower power voltage line VSS1 and the second lower power voltage line VDD1 may overlap the fan-out wiring FL. In an exemplary embodiment, both of the first lower power voltage line VSS1 and the second lower power voltage line VDD1 may overlap the fan-out wiring FL. Furthermore, a gap between the first lower power voltage line VSS1 and the second lower power voltage line VDD1 may overlap the fan-out wiring FL in a plan view.

[0112] The first source metal pattern may have a single-layer structure or a multiple-layer structure. In an exemplary embodiment, the first source metal pattern may have a multiple-layer structure including a titanium layer and an aluminum layer.

[0113] Referring to FIG. 9, the third insulation layer 150 is formed to cover the first source metal pattern. The third insulation layer 150 may include contact holes or openings that expose the drain electrode DE, the first lower power voltage line VSS1, and the second lower power voltage line VDD1. Thereafter, a second source metal pattern is formed on the third insulation layer 150. The third insulation layer 150 may also be referred as a first via insulation layer.

[0114] The second source metal pattern may include the connection electrode CE that contacts the drain electrode DE, the source line SL, the first upper power voltage line VSS2 that contacts the first lower power voltage line VSS1, and the second upper power voltage line VDD2 that contacts the second lower power voltage line VDD1.

[0115] A width of the first upper power voltage line VSS2 may be greater than a width of the first lower power voltage line VSS1. For example, the first upper power voltage line VSS2 may have a shape extending toward the pixel area 30 in a cross-sectional view. A width of the second lower power voltage line VDD1 may be greater than a width of the second upper power voltage line VDD2. For example, the second lower power voltage line VDD1 may have a shape extending toward the first lower power voltage line VSS1 in a cross-sectional view. In an exemplary embodiment, the first upper power voltage line VSS2 may overlap at least a portion of the second lower power voltage line VDD1 in a plan view. The first upper power voltage line VSS2 may cover a gap between the first lower power voltage line VSS1 and the second lower power voltage line VDD1 in a plan view.

[0116] Referring to FIG. 10, the fourth insulation layer 160 is formed to cover the second source metal pattern. The fourth insulation layer 160 may also be referred as a second via insulation layer. The fourth insulation layer 160 may include a contact hole exposing the connection electrode CE. The fourth insulation layer 160 may extend from the pixel area 30 to the peripheral area 40 to cover the second

upper power voltage line VDD2. The fourth insulation layer 160 may include one or more dam structures. For example, the lower pattern DM1a of the first dam structure DM1 may be formed on the first upper power voltage line VSS2, and the lower pattern DM2a of the second dam structure DM2 may be formed to be spaced apart from the first dam structure DM1.

[0117] Thereafter, the first electrode EL1 of the organic light-emitting diode is formed on the fourth insulation layer 160. The first electrode EL1 may contact the connection electrode CE.

[0118] Referring to FIG. 11, the pixel-defining layer PDL is formed on the fourth insulation layer 160. The pixel-defining layer PDL includes an opening that exposes at least a portion of the first electrode EL1. Another pattern of the dam structures DM1 and DM2 may be formed in the pixel-defining layer PDL. For example, the upper pattern DM1b of the first dam structure DM1 may be formed on the lower pattern DM1a of the first dam structure DM1, and an upper pattern DM2b of the second dam structure DM2 may be formed on the lower pattern DM2a of the second dam structure DM2.

[0119] The organic light-emitting layer OL may be formed on the first electrode EL1. The second electrode EL2 may be formed on the organic light-emitting layer OL and the pixel-defining layer PDL. The second electrode EL2 may extend from the pixel area 30 to the peripheral area 40 to connect to the first upper power voltage line VSS2.

[0120] Although not illustrated, a capping layer, a blocking layer, or the like may be further formed on the second electrode EL2.

[0121] Referring to FIG. 12, the thin film encapsulation layer is formed in the pixel area 30 and the peripheral area 40. The thin film encapsulation layer may include the organic layer 172 and the inorganic layer 174.

[0122] Thereafter, as illustrated in FIG. 5, a touch screen structure including the sensing electrode TE may be formed on the thin film encapsulation layer.

[0123] FIG. 13 is a cross-sectional view illustrating an organic light-emitting display device according to an exemplary embodiment. FIG. 13 shows a cross-section taken along the line I-I' of FIGS. 3 and 4.

[0124] Referring to FIG. 13, a pixel PX disposed in the pixel area 30 includes a driving transistor that is disposed on the base substrate 110, an organic light-emitting diode that is electrically connected to the driving transistor, and a thin film encapsulation layer that covers the organic light-emitting diode.

[0125] The fan-out wiring FL, the first power voltage wiring VSS, the second power voltage wiring VDD, the first dam structure DM1, and the second dam structure DM2 may be disposed in the peripheral area 40 that surrounds the pixel area 30.

[0126] The organic light-emitting display device illustrated in FIG. 13 may have substantially same configuration as the organic light-emitting display device 100 illustrated in FIG. 5 except for a connection structure of an upper layer and a lower layer of the power voltage wirings VSS and VDD. Thus, any duplicated explanation may be omitted.

[0127] Referring to FIG. 13, the first power voltage wiring VSS includes the first lower power voltage line VSS1 and the first upper power voltage line VSS2. The first upper power voltage line VSS2 is disposed on the first lower power voltage line VSS1. The first upper power voltage line VSS2

may pass through a plurality of contact holes formed in the third insulation layer 150 to connect to the first lower power voltage line VSS1.

[0128] The second power voltage wiring VDD includes the second lower power voltage line VDD1 and the second upper power voltage line VDD2. The second upper power voltage line VDD2 may pass through a contact hole formed in the third insulation layer 150 to connect to the second lower power voltage line VDD1. In another example embodiment, the second upper power voltage line VDD2 may be electrically connected to the second lower power voltage line VDD1 via a plurality of contact holes formed in the third insulation layer 150.

[0129] When the upper layer and the lower layer does not form a continuous contact interface but are connected through one or more contact holes, contamination or a damage to a pixel circuit due to static electricity may be reduced or prevented.

[0130] FIG. 14 is a cross-sectional view illustrating an organic light-emitting display device according to an exemplary embodiment. FIG. 14 shows a cross-section taken along the line I-I' of FIGS. 3 and 4.

[0131] Referring to FIG. 14, a pixel PX disposed in the pixel area 30 includes a driving transistor that is disposed on the base substrate 110, an organic light-emitting diode that is electrically connected to the driving transistor, and a thin film encapsulation layer that covers the organic light-emitting diode.

[0132] The fan-out wiring FL, the first power voltage wiring VSS, the second power voltage wiring VDD, the first dam structure DM1, the second dam structure DM2 and a valley structure VS may be disposed in the peripheral area 40 that surrounds the pixel area 30.

[0133] The organic light-emitting display device illustrated in FIG. 14 may have substantially same configuration as the organic light-emitting display device illustrated in FIG. 13 except for a valley structure VS. Thus, any duplicated explanation may be omitted.

[0134] Referring to FIG. 14, the valley structure VS may be disposed between the first dam structure DM1 and the pixel area 30. For example, the valley structure VS may be disposed between the first dam structure DM1 and an end of the fourth insulation layer 160 and may be disposed on the first upper power voltage line VSS2. The valley structure VS may extend in the same direction as the dam structures DM1 and DM2.

[0135] The second electrode EL2 of the organic light-emitting diode may extend along an upper surface and a side surface of the valley structure VS. The organic layer 172 of the thin film encapsulation layer may cover the valley structure VS.

[0136] The valley structure VS may have a stack structure including a lower pattern VSa and an upper pattern VSb. The lower pattern VSa may be formed in the same layer as the fourth insulation layer 140, and the upper pattern VSb may be formed in the same layer as the pixel-defining layer PDL. The valley structure VS may increase a size of a wetting area for monomers provided thereon, and may form a valley between the valley structure VS and the end of the fourth insulation layer 160. Thus, reflowing of the monomers may be controlled in the process of forming the organic layer 172 of the thin film encapsulation layer.

[0137] As desired, a plurality of the valley structures VS may be disposed.

[0138] In an exemplary embodiment, the first upper power voltage line VSS2 may include at least one contact hole. The lower pattern VSa of the valley structure VS may be connected to the third insulation layer 150 through the contact hole.

[0139] The contact hole of the first upper power voltage line VSS2 may improve outgassing in the process of curing a via insulation layer. Furthermore, when the lower pattern VSa of the valley structure VS is connected to the third insulation layer 150, separation or lifting of the valley structure VS may be prevented in a developing process.

[0140] Exemplary embodiments of the present inventive concept may be applied to various display devices that may be used for an automobile, a vessel, an aircraft, a mobile communication device, a display device for exhibition or information delivery, a medical display device, a home appliance, or the like.

[0141] The foregoing is illustrative of exemplary embodiments and is not to be construed as limiting thereof. Although exemplary embodiments have been described, those skilled in the art will readily appreciate that many modifications are possible in the exemplary embodiments without materially departing from the novel teachings and aspects of the present inventive concept. Accordingly, such modifications are intended to be included within the scope of the present inventive concept. Therefore, it is to be understood that the foregoing is illustrative of various exemplary embodiments and is not to be construed as limited to the specific exemplary embodiments disclosed, and that modifications to the disclosed exemplary embodiments, as well as other exemplary embodiments, are intended to be included within the scope of the present inventive concept, as set forth in the following claims and equivalents thereof.

What is claimed is:

1. An organic light-emitting display device comprising:
 - a base substrate including a pixel area and a peripheral area that surrounds the pixel area;
 - a pixel array disposed in the pixel area;
 - a first power voltage wiring disposed in the peripheral area and including a first lower power voltage line and a first upper power voltage line, wherein the first upper power voltage line is disposed on the first lower power voltage line and contacts the first lower power voltage line; and
 - a second power voltage wiring disposed in the peripheral area and including a second lower power voltage line and a second upper power voltage line, wherein the second upper power voltage line is disposed on the second lower power voltage line and contacts the second lower power voltage line,
 wherein the first upper power voltage line overlaps the second lower power voltage line in a plan view.
2. The organic light-emitting display device of claim 1, wherein the second power voltage wiring is disposed between the first power voltage wiring and the pixel area.
3. The organic light-emitting display device of claim 2, wherein the first lower power voltage line is spaced apart from the second lower power voltage line, and the first upper power voltage line is spaced apart from the second upper power voltage line.
4. The organic light-emitting display device of claim 3, wherein a width of the first upper power voltage line is greater than a width of the first lower power voltage line, and

a width of the second upper power voltage line is smaller than a width of the second lower power voltage line.

5. The organic light-emitting display device of claim 3, wherein the first upper power voltage line covers a gap between the first lower power voltage line and the second lower power voltage line in a plan view.

6. The organic light-emitting display device of claim 1, wherein the pixel array includes an organic light-emitting diode that includes a first electrode and a second electrode, wherein the second electrode of the organic light-emitting diode extends from the pixel area to the peripheral area and contacts the first upper power voltage line.

7. The organic light-emitting display device of claim 1, further comprising a fan-out wiring overlapping the first power voltage wiring and the second power voltage wiring.

8. The organic light-emitting display device of claim 7, wherein the fan-out wiring is disposed under the first power voltage wiring and the second power voltage wiring.

9. The organic light-emitting display device of claim 8, wherein the fan-out wiring includes a plurality of lines spaced apart from each other, wherein at least a portion of the fan-out wiring overlaps a gap between the first lower power voltage line and the second lower power voltage line in a plan view.

10. The organic light-emitting display device of claim 7, further comprising a touch screen structure disposed in the pixel area and the peripheral area to overlap the fan-out wiring.

11. The organic light-emitting display device of claim 1, wherein the fan-out wiring is configured to transfer a data signal to the pixel array.

12. The organic light-emitting display device of claim 1, further comprising a first via insulation layer partially covering the first lower power voltage line and the second lower power voltage line.

13. The organic light-emitting display device of claim 12, wherein the first via insulation layer includes one or more contact holes, and the first upper power voltage line is connected to the first lower power voltage line through the one or more contact holes of the first via insulation layer.

14. The organic light-emitting display device of claim 12, wherein the first via insulation layer includes one or more contact holes, and the second upper power voltage line is connected to the second lower power voltage line through one or more contact holes of the first via insulation layer.

15. The organic light-emitting display device of claim 1, further comprising a thin film encapsulation layer covering the pixel array and extending to the peripheral area.

16. The organic light-emitting display device of claim 15, wherein the thin film encapsulation layer includes at least one organic layer and at least one inorganic layer.

17. The organic light-emitting display device of claim 16, further comprising at least one dam structure disposed in the peripheral area.

18. The organic light-emitting display device of claim 17, further comprising at least one valley structure disposed between the at least one dam structure and the pixel area.

19. The organic light-emitting display device of claim 18, wherein the pixel array includes an organic light-emitting diode that includes a first electrode and a second electrode, wherein the second electrode of the organic light-emitting diode is disposed in the pixel area and the peripheral area, extends along a side surface and an upper surface of the at

least one valley structure in the peripheral area, and contacts the first upper power voltage line.

20. The organic light-emitting display device of claim **18**, wherein the at least one valley structure is disposed on the first upper power voltage line and is connected to a first via insulation layer that is disposed under the first upper power voltage line through a contact hole of the first upper power voltage line.

* * * * *

专利名称(译)	有机发光显示装置		
公开(公告)号	US20190341439A1	公开(公告)日	2019-11-07
申请号	US16/377255	申请日	2019-04-08
[标]申请(专利权)人(译)	三星显示有限公司		
申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
[标]发明人	CHOI YOONSUN LEE SEONG RYONG KIM HYUN CHUL LEE SEONGJUN JUNG EUNAE		
发明人	CHOI, YOONSUN LEE, SEONG RYONG KIM, HYUN CHUL LEE, SEONGJUN JUNG, EUNAE		
IPC分类号	H01L27/32 H01L51/52 G09G3/3291		
CPC分类号	H01L51/5256 G09G2300/0426 G09G2300/0439 H01L27/3246 G09G3/3291 H01L27/323 H01L27/3276 G09F9/301 H01L2227/323		
优先权	1020180052158 2018-05-04 KR		
外部链接	Espacenet USPTO		

摘要(译)

有机发光显示装置包括基底，像素阵列，第一电源电压布线和第二电源电压布线。基底基板包括像素区域和围绕像素区域的外围区域。像素阵列设置在像素区域中。第一电源电压布线设置在外围区域中，并且包括第一下部电源电压线和第一上部电源电压线。第一上电源电压线设置在第一下电源电压线上并与第一下电源电压线接触。第二电源电压布线设置在外围区域中，并且包括第二下部电源电压线和第二上部电源电压线。第二上电源电压线设置在第二下电源电压线上并与第二下电源电压线接触。在平面图中，第一上部电源电压线与第二下部电源电压线重叠。

